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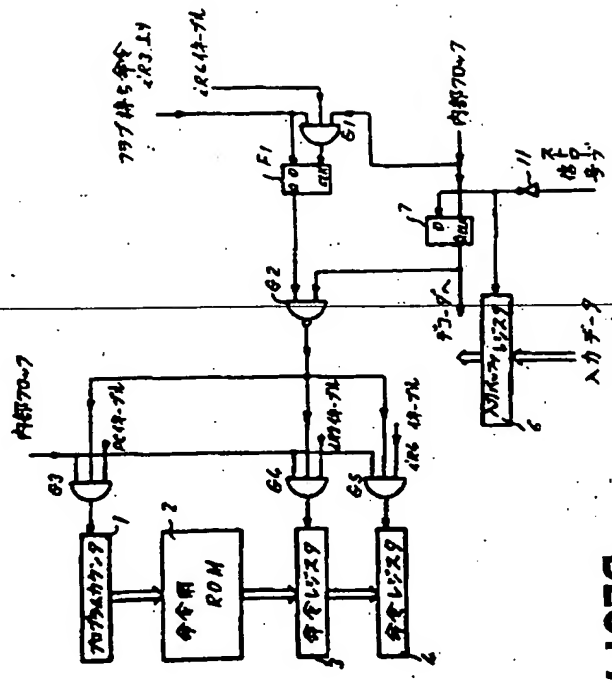
TITLE : SIGNAL PROCESSING SYSTEM



ABSTRACT : PURPOSE: To execute the next program at a high speed by providing a flag waiting instruction to discontinue the clocks to be applied to a program counter and an instruction register and a means which supplies the clocks to said counter and register when the input data flag is changed.

CONSTITUTION: A program counter PC1 and instruction registers iR3 and 4 are in an enable state respectively, and the internal processing is through with an input buffer register 6. Then a flag waiting instruction is delivered from an ROM2 when the next input signal is accepted and then supplied to a decoder 5 through the register iR4. The output Q of an FFF_1 is set at "1". When a strobe signal is set at "H" level after the input of the input data is over to the register 6, the output of an FF7 for input data flag is set at "0". While the output of an NAND circuit G2 is set at "1", and the internal clocks are simultaneously supplied to the counter PC1 and registers iR3 and 4 to advance the program. On the contrary, the program has no progress in case the input data is not completely fed into the register yet with the strobe signal set at "L" level respectively.